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Application Note

Design Considerations When Using the HI1176 Input Clamp Circuit

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Introduction

The HI1176 is an 8-bit CMOS analog-to-digital converter designed for video applications and includes a sync clamp function. The device utilizes a 2-step parallel conversion method which allows for high conversion speeds and low power consumption. The datasheet for the HI1176 can be obtained by accessing AnswerFAX document number 3582.

Clamp Operation

The HI1176 has the capability to clamp the input signal before it is digitized by the ADC (see Figure 1). A comparator is used to determine if the input, during the clamp pulse time, is above or below the desired clamp voltage, V_{REF}. Once the comparison has been made, the appropriate current source is then turned on to charge the input capacitor up or down depending on the comparator output. The HI1176 also has an internal monostable multivibrator that can be set to run in various modes of clamp pulse operation. For example, if performing the DC restore function for NTSC video, the HI1176 can be configured to clamp the back porch of the incoming video to the voltage on the V_{REF} pin. If a sync detect function is required after the ADC, then V_{REF} can be set so the complete video signal including the sync pulse is digitized. If the sync is to be stripped before the ADC then V_{REF} can be set so only the active video portion of the video gets digitized. This will effectively increase the resolution for this portion of the video signal.

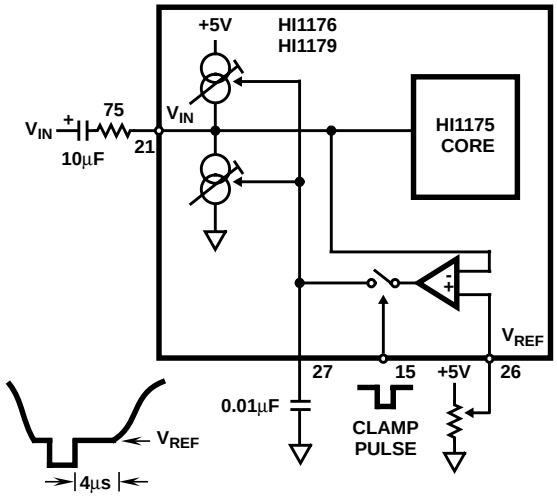
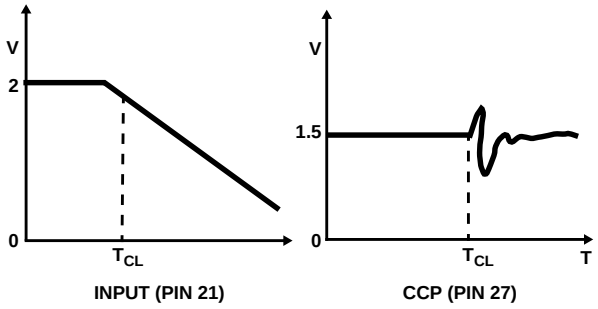


FIGURE 1. CLAMP BLOCK DIAGRAM

There are several methods for implementing the input DC restore function when using the HI1176. One method is to directly input the clamp pulse. Another method is to use the internal monostable multivibrator, eliminating the external monostable multivibrator. To use the built in multivibrator an RC network is necessary to set the pulse width on pin 15 and the clamping pulse is connected to pin 14 (SYNC). An RC of 130k and 100pF gives a 2.75µs pulse. Narrower pulse widths can be achieved by reducing the resistor and/or capacitor values. The SEL pin (pin 13) will determine which SYNC edge the pulse is generated on. In this mode of operation, the RC time constant can be set to provide very narrow pulse widths. As a general rule, the resistor value should be a minimum of 5k and capacitance should be greater than zero (the monostable will generally work without a capacitor connected due to parasitic capacitance provided by the package, bond wires and silicon itself, however this is not recommended due to lot variation in the assembly and wafer fab processes).

The minimum reset time for the monostable is equal to one period of the sampling clock (or 50ns for 20MHz operation).



T_{CL} = CLAMP PULSE OCCURRENCE

FIGURE 2. CLAMPING CHARACTERISTICS

When inputting the clamp pulse directly, care should be taken to have the SYNC pulse input latched by the ADC sampling clock connected to the PW input. This is done to prevent beat frequencies, generated between the clock and clamp inputs, from showing up as vertical sag in video applications. If this is not a concern the latch is not necessary. In this mode of operation, narrow pulse widths can also be achieved. The minimum allowable pulse on the PW pin (14) in this configuration is 1.75ns. Figure 3 graphically illustrates this mode of operation.

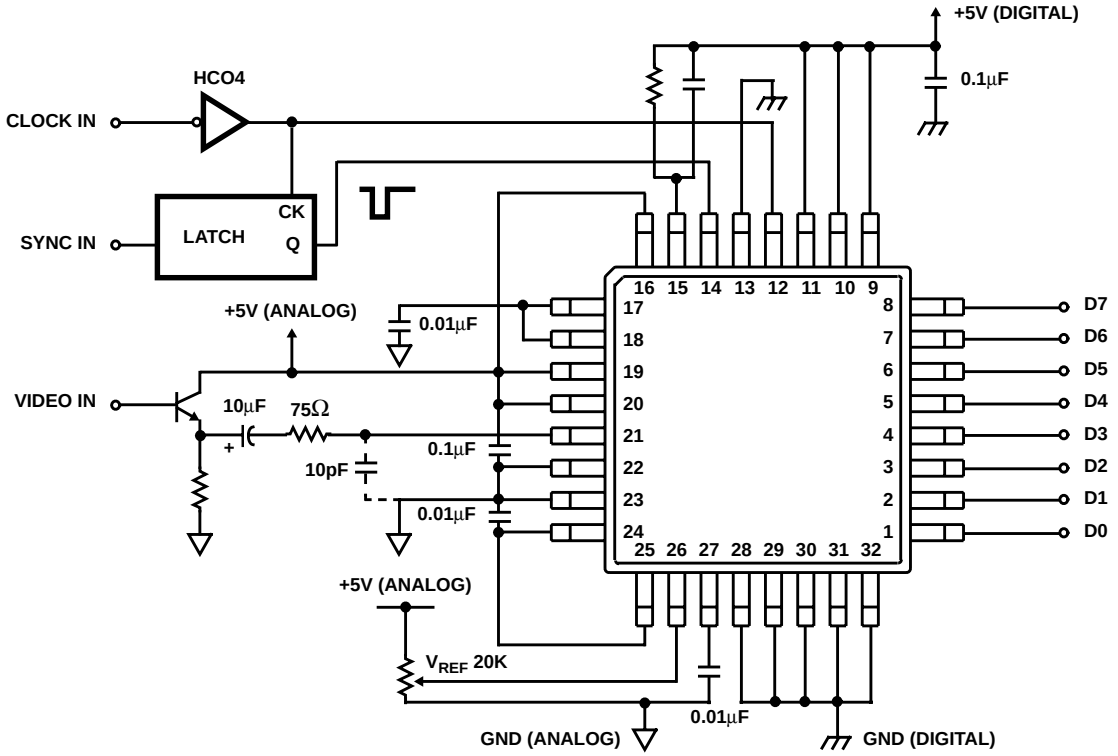


FIGURE 3. PEDESTAL CLAMP EXECUTED BY SYNC PULSE

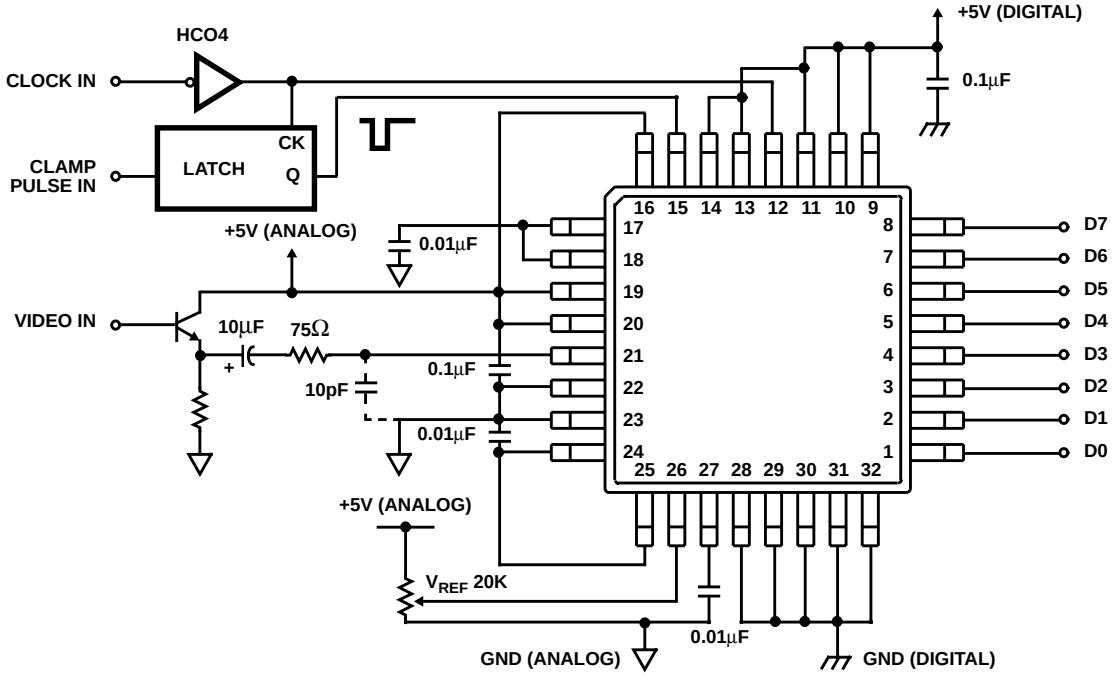


FIGURE 4. CLAMP PULSE IS DIRECTLY INPUT (SELF BIAS USED)

Design Equations

As stated in the previous section, the HI1176 clamp circuitry gives designers the ability to clamp the ADC input to a predetermined value set by the voltage on the V_{REF} pin. When enabled, the clamp circuit (as seen in Figure 5) closes the feedback loop to the input and thereby calling in a low pass filter function defined by the following equation:

$$F_C = \frac{1}{\left(1 + j\omega CR \times \frac{(T_S)}{(T_{PW})}\right)}$$

Where T_S is the period of the clamp pulse, t_{PW} is width of the clamp pulse, R is the output resistance of the comparator (typically 2kΩ) and C is the C_{CP} capacitor on pin 27 of the HI1176 (nomenclature changed to avoid confusion during analysis).

Typical values for the variables in the equation above are as follows:

R = 2kΩ, C = 0.01µF, T_S = 15µs, T_{PW} = 2ns.

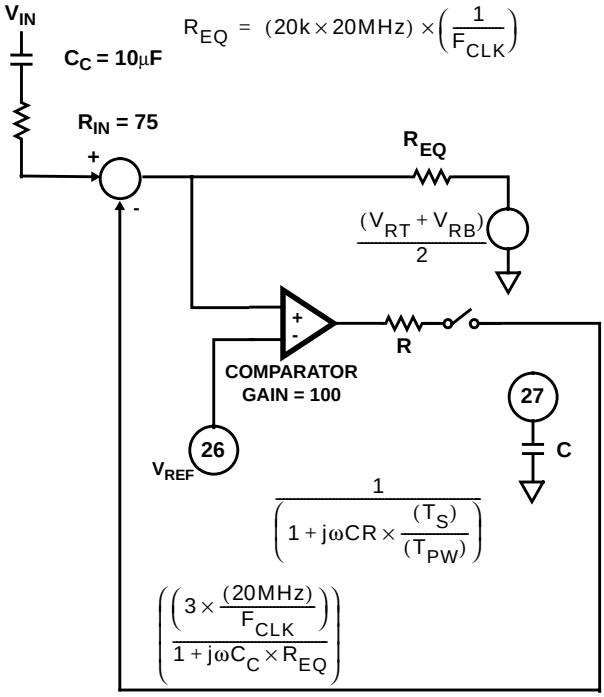
Inserting these values and solving for the cutoff frequency of the low pass filter yields a cutoff frequency for the low-pass which will effectively filter out the desired signal.

$$F_C = \frac{1}{1 + 2\pi\,(0.01\mu F)\,(100)\,\frac{(15\mu s)}{(2ns)}} = 0.955Hz$$

The overall equation for the ADC can also be solved for in a similar fashion. By using the equation defined in Figure 5 for the overall feedback loop, a cutoff frequency of 1.32Hz is obtained at a sampling frequency of 20MHz.

Conclusion

The input clamp circuit of the HI1176 has been shown to be a useful tool for users who wish to select portions of their incoming signals which they do not wish to digitize. The flexibility of the circuit makes it ideally suited for a variety of applications, particularly those which are video related. Should your application require faster sampling speeds than the HI1176 offer, refer to the HI1179 (datasheet available via AnswerFAX document 3566). The HI1179 offers a similar input clamp circuit to the HI1176 and is capable of sampling speeds up to 35MHz.



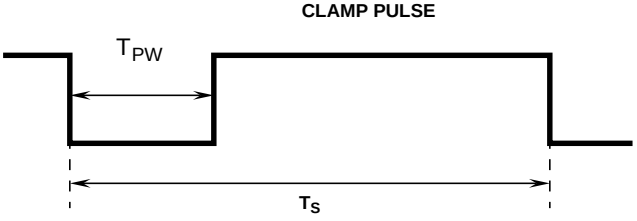


FIGURE 5. CHARACTERISTIC EQUATIONS DEFINING CLAMP FUNCTION.

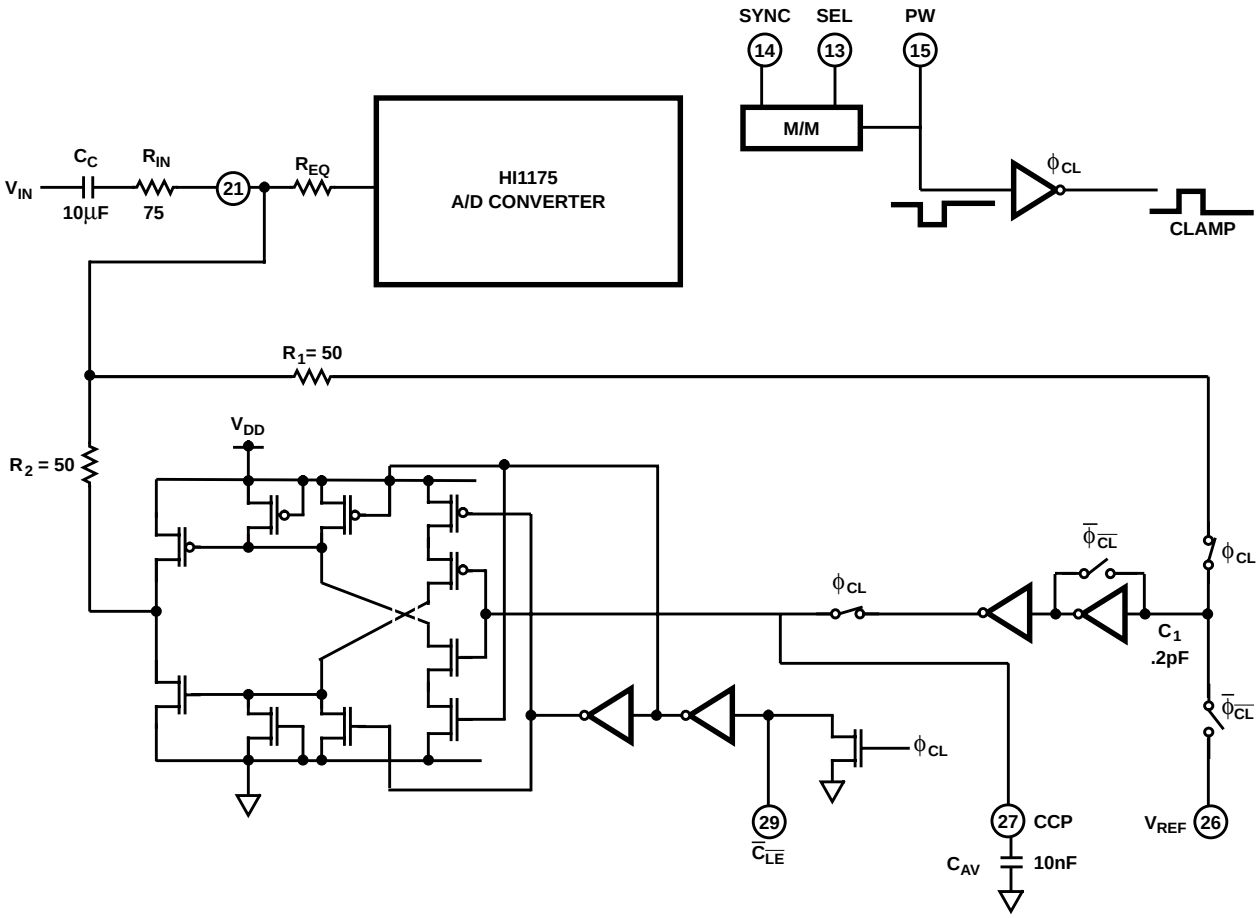


FIGURE 6. CLAMP CIRCUIT HI1176

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